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	INFORMATION D			Application Number	10/577,398	
	STATEMENT BY	APPLI	CANT	Filing Date	09/17/2004	
	Date Submitted: N	May 23	2006	First Named Inventor	Koichi TAKEDA	
				Group Art Unit	Unassigned	
	(use as many sheets	s as ne	cessary)	Examiner Name	Unassigned	
Sheet	1	of	1	Attorney Docket Number	016778-0507	

U.S. PATENT DOCUMENTS									
Examiner Initials*	Cit-	U.S. Patent Document			Date of Publication of	Pages, Columns, Lines,			
	Cite No. <sup>1</sup>	Number	Kind Code <sup>2</sup> (if known)	Name of Patentee or Applicant of Cited Document	Cited Document  MM-DD-YYYY	Where Relevant Passages or Relevant Figures Appear			

			U.S	. PATENT APPLICATION DOCU	MENTS	
Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Application Document		Name of Datastan . A. II	Filing Date of	Pages, Columns, Lines, Where Relevant
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		NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.				
	B1	A.J. BHAVNAGARWALA et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," IEEE Journal of Solid-State Circuits, Vol. 36:4, April, 2001.				
	B2	H. SAKAKIBARA et al., "A 750 MHz Cache DRAM LSi with Speed Scalable Design and Programmable at- Speed Function-Array BIST," 2003 IEEE International Solid-State Circuits Conference				

Examiner Signature	/Son Mai/	Date Considered	06/25/2008

<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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